CLAIM AMENDMENTS

What is claimed is:

1. (currently amended) A debugging system, comprising:

a processor constructed to execute a software ~~process~~ program;

a fast-response circuit coupled to a low-level asset in the processor;

the fast response circuit configurable to extract selectively data from the low-level asset without major time-distortion of the software program executing on the processor; and

a data path ~~extending from the fast response circuit and~~ constructed to transfer ~~transmit~~ extracted ~~evidence~~ sustained data to an evidence file.

2. (currently amended) A debugging system, comprising:

a processor constructed to execute a software ~~process~~ program;

a fast-response circuit coupled to a low-level asset in the processor;

the fast response circuit configurable to monitor selectively sustained data from the low level asset for a predetermined event without major time-distortion of the software program executing on the processor; and

~~an action line extending from~~ wherein the fast response circuit is ~~and~~ constructed to transmit an action signal responsive to the event.

3. (currently amended) A debugging system, comprising:

a processor constructed to execute a software ~~process~~ program;

a fast-response circuit coupled to a low-level data asset in the processor;

the fast response circuit having a first portion configurable to monitor data from the low level asset for a predetermined event, and constructed to generate an action signal upon the occurrence of the predetermined event;

the fast response circuit having a second portion configurable to extract selectively data from the low-level asset, and constructed to act responsive to the action signal; and

a data path ~~extending from the fast response circuit and~~ constructed to transmit extracted ~~evidence~~ sustained data to an evidence file without major time-distortion of the software program executing on the processor .

4. (original) The debugging system of claim 1, 2, or 3, wherein the low-level asset is constructed as a commit buffer, a reorder buffer, a high speed data bus, or a register.

5. (original) The debugging system of claim 1, 2, or 3 wherein the fast response circuit is integrated on-chip with the low-level asset of the processor.

6. (original) The debugging system of claim 1, 2, or 3, wherein the fast response circuit comprises high speed registers.

7. (currently amended) The debugging system of claim 1, 2, or 3, wherein the data path comprises one or more resources of the processor's hierarchy. ~~is a high speed bus extending from the fast response circuit to a cache on-chip with the processor.~~

8. (currently amended) The debugging system according to claim 3, further including:

sequential logic connected to the first portion of the fast response circuit; and

wherein the sequential logic is programmable to selectively monitor for ~~compound process~~ program events, and the sequential logic enables an action responsive to the ~~compound process~~ program events.

9. (currently amended) The debugging system according to claim 3, further including:

sequential logic connected to the second portion of the fast response circuit; and

wherein the sequential logic is programmable to selectively extract data ~~according to compound criteria~~.

10. (original) The debugging system according to claim 8 or 9, wherein the sequential logic is constructed as a co-processor.

11. (original) The debugging system according to claim 8 or 9, wherein the sequential logic is integrated on-chip with the low-level asset of the processor.

12. (currently amended) A processor chip, comprising:

a low-level asset;

a fast-response circuit coupled to the low-level asset;

the fast response circuit having a first portion configurable to monitor data from the low level asset for a predetermined event, and constructed to generate an action signal upon the occurrence of the predetermined event;

the fast response circuit having a second portion configurable to extract selectively data from the low-level asset, and constructed to act responsive to the action signal; and

a data path including one or more resources of the processor's hierarchy ~~extending from the fast response circuit to a cache memory~~, the data path constructed to transmit ~~extracted~~ sustained evidence data to an evidence file.

13. (cancelled)

14. (currently amended) A processor comprising:

a low level asset;

a fast response circuit preconfigured to monitor for an event and to extract data selectively;

a high-speed data path constructed to transfer ~~transmit~~ sustained data from the low level asset to the fast response circuit;

wherein the processor performs the steps of:

~~pre-configuring the fast response logic to monitor for an event~~

~~pre-configuring the fast response logic to extract data selectively;~~

executing a central-program;

detecting the event using the fast response logic;

extracting data selectively using the fast response logic; and

transferring the extracted data to a ~~cache~~ memory; and

wherein the detecting, extracting, and transferring steps are performed without major time-distortion of the central program executing on the processor.

15. (original) The processor according to claim 14, further comprising:

a second low-level asset connected to the fast response circuit; and

wherein the extracting step includes selectively extracting data from the second low-level asset.

16. (original) The processor according to claim 14, further comprising:

a sequential logic circuit connected to the fast response circuit; and

wherein the processor performs the steps of:

transmitting an action signal to the sequential logic responsive to detecting the event.

17. (cancelled)

18. (cancelled)

19. (new) A debugging system, comprising:

a processor constructed to execute a software program and having a shared high-speed data transfer bus;

a fast-response circuit coupled to a low-level asset in the processor;

the fast response circuit configurable to extract sustained data from the low-level asset; and

a high-speed data path extending to an evidence file, the high-speed data path including the shared high-speed data transfer bus.

20. (new) The debugging system according to claim 19, wherein the high speed data path further includes one or more resources of the processor's hierarchy.

21. (new) The debugging system according to claim 19, wherein the fast response circuit is constructed to extract the sustained data without major time-distortion to the software program executing on the processor .

22. (new) The debugging system according to claim 19, wherein the high-speed data path is constructed to transfer the sustained data to the evidence file without major time-distortion to the software program executing on the processor .